Devanshu Sanjiv Gajjar

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EDUCATION

San Jose State University, *M.S., in Electrical and Electronics Engineering* | San Jose, USA | GPA 3.9/4.0 Dec 2025

Nirma University*, Bachelor of Technology in Electronics & Communication Engineering* | Ahmedabad, India May 2021

*Courses***:** *Advance Computer Architecture, Advance Digital System Design and Synthesis, Digital Communication, Data Structure, Modern Processor Architecture*

WORK EXPERIENCE

Einfochips Pvt Ltd, India **| Embedded Engineer** Aug 2021 – Dec 2023

- Created an integrated software and firmware for a battery management system built into a security system, utilizing an **ARM Cortex M4** and **A7**.
- Programmed and verified different protocols such as I2C, SPI, and UART on the **STM32L475** Discovery Board with ARM **Cortex M4** applying BareMetal coding.
- Simulated a finite state machine for SPI to simulate individual block functionality using **System C**.
- Developed an application for the **FTDI FT2322H** (USB 2.0 to JTAG Convertor) using the PyFTDI module in **Python**.
- Managing 3-person team delivering **JTAG** protocol employed on **RPI Pico**, resulting in a cost reduction of 50% for customers while maintaining same functionality with more affordable technology.
- Engineered a system application for communication and debugging over serial wire JTAG offering different functionality on the **ARM SoC 600**.
- Initiated software Module and Driver development on Renesas RX65n microcontroller and porting from Renesas **RX231** to **RX65n**.

ACADEMIC PROJECTS

UART Controller with FIFO Buffer Function based on AXI-Lite Jan 2024 – May 2024

Dr. Bin Le, San Jose State University

- Developed a UART Controller with FIFO Buffer, based on **AXI Lite** in **System Verilog**, and implemented on a **Xilinx Nexys 7** FPGA for communication between high speed and low speed devices.
- Engineered IP integration with Xilinx's **MicroBlaze**; mitigated UART device monopolization of the AXI bus, leading to a 20% improve ment in data throughput and a 10% reduction in system bottlenecks.
- Conducted comprehensive Static Timing Analysis using **PrimeTime**, ensuring the design met all timing requirements and constraints for optimal performance and reliability.

MIPS (ISA) with Forward Chaining and 2-Bit Branch Predictor Jan 2024 – May 2024

Dr. Chang Choo, San Jose State University

- Demonstrated 5 stage MIPS ISA in **Verilog**, equipped with forward chaining, effectively resolves data and control hazards, thereby reducing clock cycles and enhancing performance.
- Computed branch prediction accuracy using 2-bit branch predictor reducing the number of waste cycles by 46%.

Cache Simulator Jan 2024 – May 2024

Dr. Chang Choo, San Jose State University

- Implemented a data cache simulator for m-way set-associative caches, supporting block sizes ranging from 32 to 256B and cache sizes up to 128KB.
- Simulated in **Python** using LRU, FIFO and Random Cache Replacement Algorithm.
- Analyzed simulation results and generated graphs to evaluate cache miss rates while varying cache parameters.

SKILLS & COMPETENCIES

Programming Languages: C, Python, System C, Shell and Bash Scripting, GIT, Verilog, System Verilog, UVM.
Hardware Technologies: STM32, Renesas RX231, RX65n, FTDI FT2322, ARM Cortex M4, A7, Nexys A7 FPGA.
Tools: MATLAB, STM32 Cube IDE, Vivado (Xilinx), Vitis (Xilinx), Quartus (Intel), Proteus, NI ModelSim, PrimeTime (Synopsys), Design Compiler, Design Vision.
Bus Protocols: AMBA AXI, APB, SPI, I2C, UART
Instruments: Saleae Logic Analyzer, ST-Link, Aardvark, Spectrum Analyzer.

PUBLICATIONS

Devanshu Gajjar, Divyesh Sankhla, Jagrat Jhamb, Industrial Automation Using PLC, and IoT Advancements, IJERT,2021 (Manuscript Accepted)